The documentation and process conversion measures necessary to comply with this revision shall be completed by 7 July 2004.

IINCH-POUND

MIL-PRF-19500/592E
7 April 2004
SUPERSEDING
MIL-PRF-19500/592D
29 May 2003

PERFORMANCE SPECIFICATION SHEET

* SEMICONDUCTOR DEVICE, REPETITIVE AVALANCHE, FIELD EFFECT TRANSISTOR, N-CHANNEL, SILICON, TYPES 2N7224, 2N7225, 2N7227, 2N7228, 2N7224U, 2N7225U, 2N7227U, AND 2N7228U, JAN, JANTX, JANTXV, JANS, JANHC, AND JANKC

This specification is approved for use by all Departments and Agencies of the Department of Defense.

* The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

* 1.1 Scope. This specification covers the performance requirements for an N-channel, enhancement-mode, MOSFET, power transistor intended for use in high density power switching applications. Four levels of product assurance are provided for each encapsulated device type as specified in MIL-PRF-19500, and two levels of product assurance for each unencapsulated device type die, with avalanche energy ratings (E_{AS} and E_{AR}) and maximum avalanche current (I_{AR}).

1.2 Physical dimensions. See figure 1 (TO-254AA), figure 2 (TO-276AB, surface mount), and figure 3 for JANHC and JANKC (die) dimensions.

* 1.3 Maximum ratings. (T_A = +25°C, unless otherwise specified).

Type	P_T (1) T_C = +25°C	P_T T_A = +25°C	V_{GS}	I_{D1} (2) (3) T_C = +25°C	I_{D2} (2) T_C = +100°C	I_S	I_{DM} (4)	T_J and T_{STG}	V_{ISO} at 70,000 foot	$R_{\theta JC}$ max
	W	W	V dc	A dc	A dc	A dc	A(pk)	°C		°C/W
2N7224, 2N7224U	150	4.0	±20	34.0	21	34.0	136	-55		0.83
2N7225, 2N7225U	150	4.0	±20	27.4	17	27.4	110	to		0.83
2N7227, 2N7227U	150	4.0	±20	14.0	9	14.0	56	+150	400	0.83
2N7228, 2N7228U	150	4.0	±20	12.0	8	12.0	48		500	0.83

See notes on next page.

* Comments, suggestions, or questions on this document should be addressed to Defense Supply Center, Columbus, ATTN: DSCC-VAC, P.O. Box 3990, Columbus, OH 43216-5000, or emailed to Semiconductor@dscc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at http://www.dodssp.daps.mil/.

* 1.3 Maximum ratings - Continued.

Type	I_{AR}	E_{AS}	E_{AR}	$r_{DS(on)}$ max (1) (5) V_{GS} = 10 V dc $I_D = I_{D2}$	
				T_J = +25°C	T_J = +150°C
	A	mj	mj	Ω	Ω
2N7224, 2N7224U	34.0	150	15.0	0.070	0.133
2N7225, 2N7225U	27.4	500	15.0	0.100	0.200
2N7227, 2N7227U	14.0	700	15.0	0.315	0.693
2N7228, 2N7228U	12.0	750	15.0	0.415	0.913

(1) Derate linearly 1.2 W/°C for T_C > +25°C.
(2) The following formula derives the maximum theoretical I_D limit. I_D is limited by package and internal wires and may be limited by pin diameter:

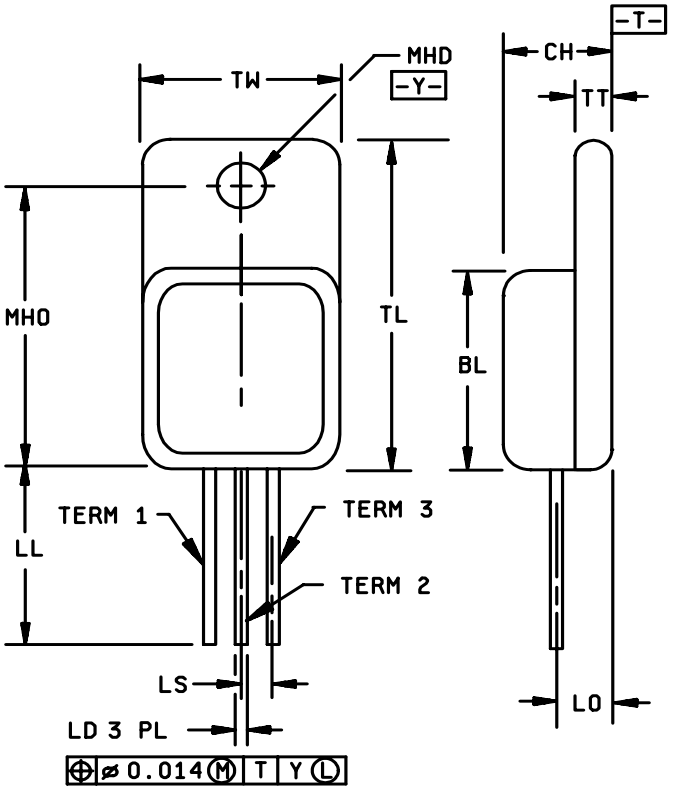
$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS}(on) \text{ at } T_{JM})}}$$

(3) See figure 4, maximum drain current graph.
(4) I_{DM} = 4 X I_{D1} as calculated in note (2).
(5) Pulsed (see 4.5.1).

1.4 Primary electrical characteristics. T_C = +25°C (unless otherwise specified).

Type	Min $V_{(BR)DSS}$ V_{GS} = 0 I_D = 1.0 mA dc	$V_{GS(th)1}$ $V_{DS} \geq V_{GS}$ I_D = 0.25 mA		Max I_{DSS1} V_{GS} = 0 V_{DS} = 80 percent of rated V_{DS}	Max $r_{DS(on)}$ (1) V_{GS} = 10 V dc $I_D = I_{D2}$ T_J = +25°C
	V dc	V dc		µA dc	Ohms
		Min	Max		
2N7224, 2N7224U	100	2.0	4.0	25	0.070
2N7225, 2N7225U	200	2.0	4.0	25	0.100
2N7227, 2N7227U	400	2.0	4.0	25	0.315
2N7228, 2N7228U	500	2.0	4.0	25	0.415

(1) Pulsed (see 4.5.1).

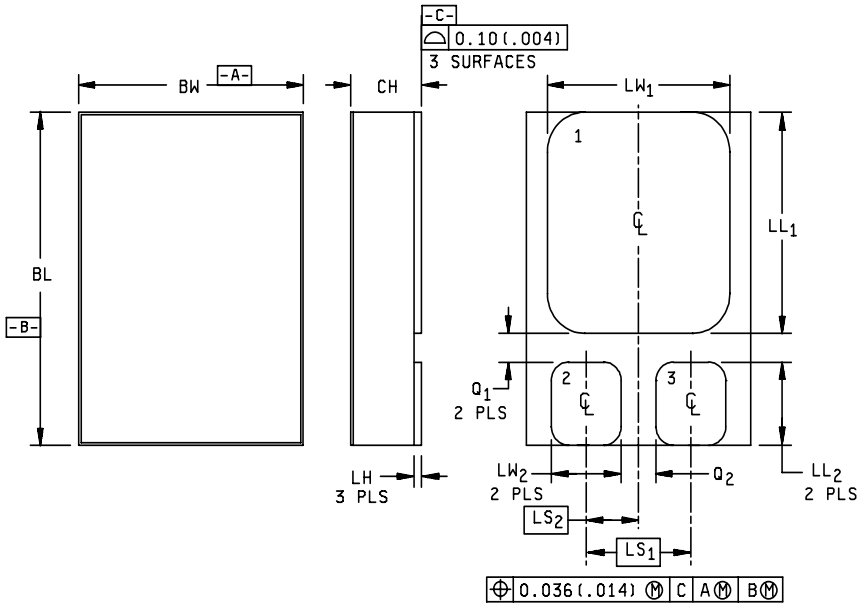


NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Glass meniscus included in dimension D and E.
4. All terminals are isolated from the case.
5. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 1. Physical dimensions for TO-254AA.

Ltr.	Dimension				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
BL	.535	.545	13.59	13.84	
CH	.249	.260	6.32	6.60	
LD	.035	.045	0.89	1.14	
LL	.510	.570	12.95	14.48	
LO	.150 BSC		3.81 BSC		
LS	.150 BSC		3.81 BSC		
MHD	.139	.149	3.53	3.78	
MHO	.665	.685	16.89	17.40	
TL	.790	.800	20.07	20.32	3, 4
TT	.040	.050	1.02	1.27	
TW	.535	.545	13.59	13.84	3, 4
Term 1	Drain				
Term 2	Source				
Term 3	Gate				

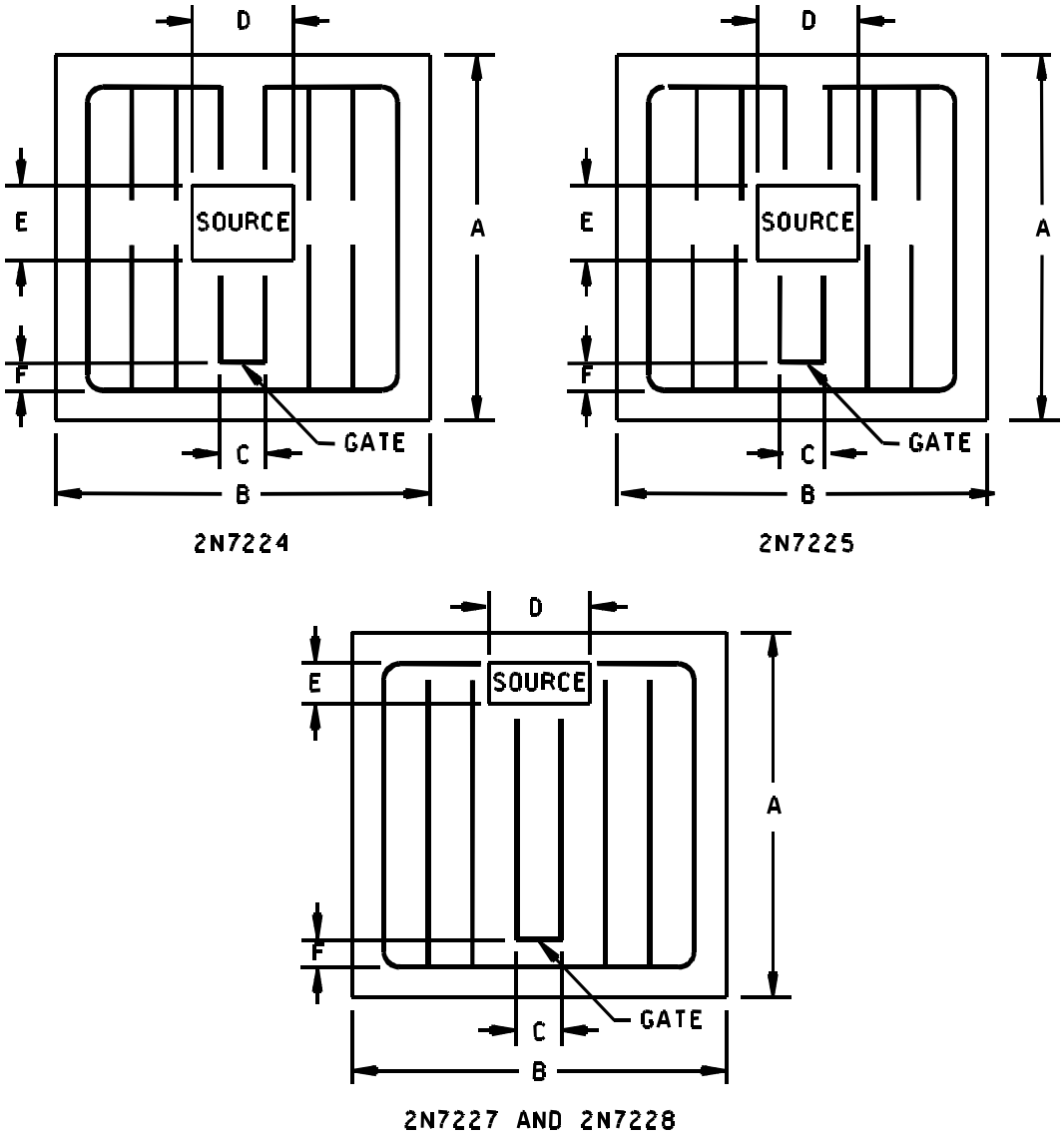
FIGURE 1. Physical dimensions for TO-254AA - Continued.



Dimensions				
Ltr.	Inches		Millimeters	
	Min	Max	Min	Max
BL	.620	.630	15.75	16.00
BW	.445	.455	11.30	11.56
CH		.142		3.60
LH	.010	.020	0.26	0.50
LL_1	.410	.420	10.41	10.67
LL_2	.152	.162	3.86	4.11
LS_1	.210 BSC		5.33 BSC	
LS_2	.105 BSC		2.67 BSC	
LW_1	.370	.380	9.40	9.65
LW_2	.135	.145	3.43	3.68
Q_1	.030		0.76	
Q_2	.035		0.89	
Term 1	Drain			
Term 2	Gate			
Term 3	Source			

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for information only.
3. The lid shall be electrically isolated from the drain, gate and source.
4. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 2. Dimensions and configuration of surface mount package outline (TO-276AB) 2N7224U, 2N7225U, 2N7227U, and 2N7228U.



NOTES:
1. Dimensions are in inches.
2. Millimeters are given for information only.
3. Unless otherwise specified, tolerance is ±.005 inches (0.13 mm).
4. Physical characteristics of the die thickness = .0187 inch (0.47 mm).
5. Back metal: Cr - Ni - Ag.
6. Top metal: Al.
7. Back contact: Drain.

FIGURE 3. Physical dimensions JANHC and JANKC.

A version

Ltr	Dimensions - 2N7224				Dimensions - 2N7225				Dimensions - 2N7227 and 2N7228			
	Inches		Millimeters		Inches		Millimeters		Inches		Millimeters	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	.252	.262	6.40	6.65	.252	.262	6.40	6.65	.252	.262	6.40	6.65
B	.252	.262	6.40	6.65	.252	.262	6.40	6.65	.252	.262	6.40	6.65
C	.027	.037	0.69	0.94	.027	.037	0.69	0.94	.025	.035	0.64	0.89
D	.066	.076	1.68	1.93	.066	.076	1.68	1.93	.043	.053	1.09	1.35
E	.047	.057	1.19	1.45	.047	.057	1.19	1.45	.032	.042	0.81	1.07
F	.013	.023	0.33	0.58	.013	.023	0.33	0.58	.015	.025	0.38	0.64

FIGURE 3. JANHC and JANKC die dimensions - Continued.

2. APPLICABLE DOCUMENTS

* 2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

* 2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

* DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

* DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://www.dodssp.daps.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in MIL-PRF-19500, and on figures 1 (TO-254AA), 2 (TO-276AB, surface mount), and 3 (die) herein. Methods used for electrical isolation of the terminal feedthroughs shall employ materials that contain a minimum of 90 percent AL_2O_3 (ceramic). Examples of such construction techniques are metallized ceramic eyelets or ceramic walled packages.

3.4.1 Lead formation, material, and finish. Lead material shall be Kovar or Alloy 52; a copper core or plated core is permitted. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead formation material or finish is desired, it shall be specified in the acquisition document (see 6.2). When lead formation is performed, as a minimum, the vendor shall perform 100-percent hermetic seal in accordance with screen 14 of table IV of MIL-PRF-19500 and 100-percent dc testing in accordance with table I, subgroup 2 herein.

3.4.2 Internal construction. Multiple chip construction shall not be permitted to meet the requirements of this specification.

3.5 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.6 Electrostatic discharge protection. The devices covered by this specification require electrostatic protection.

3.6.1 Handling. MOS devices must be handled with certain precautions to avoid damage due to the accumulation of static charge. However, the following handling practices are recommended (see 3.6).

a. Devices should be handled on benches with conductive and grounded surface.

b. Ground test equipment, tools, and personnel handling devices.

c. Do not handle devices by the leads.

d. Store devices in conductive foam or carriers.

e. Avoid use of plastic, rubber, or silk in MOS areas.

f. Maintain relative humidity above 50 percent if practical.

g. Care should be exercised, during test and troubleshooting, to apply not more than maximum rated voltage to any lead.

h. Gate must be terminated to source. $R \leq 100\ k\Omega$, whenever bias voltage is to be applied drain to source.

3.7 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I.

3.8 Electrical test requirements. The electrical test requirements shall be table I as specified herein.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500. Alternate flow is allowed for qualification inspection in accordance with MIL-PRF-19500.

4.2.1 JANHC and JANKC devices. Qualification shall be in accordance with MIL-PRF-19500.

* 4.2.2 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.3 Screening (JANTX, JANTXV, and JANS levels only). Screening shall be in accordance with table IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table IV, of MIL-PRF-19500) (1) (2)	Measurement	
	JANS level	JANTX and JANTXV levels
(3)	Gate stress (see 4.3.2)	Gate stress (see 4.3.2)
(3)	Method 3470 of MIL-STD-750 (see 4.3.3)	Method 3470 of MIL-STD-750 (see 4.3.3)
(3) 3c	Method 3161 of MIL-STD-750 (see 4.3.4)	Method 3161 of MIL-STD-750 (see 4.3.4)
7	Optional.	Optional.
9	I_{GSSF1}, I_{GSSR1}, I_{DSS1}, subgroup 2 of table herein	Subgroup 2 of table I herein.
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	Subgroup 2 of table I herein I_{GSSF1}, I_{GSSR1}, I_{DSS1}, $r_{DS(on)1}$, $V_{GS(th)1}$; ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±25 µA dc or ±100 percent of initial value, whichever is greater.	Subgroup 2 of table I herein. I_{GSSF1}, I_{GSSR1}, I_{DSS1}, $r_{DS(on)1}$, $V_{GS(th)1}$
12	Method 1042 of MIL-STD-750, condition A	Method 1042 of MIL-STD-750, condition A
13	Subgroups 2 and 3 of table I herein; ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±25 µA dc or ±100 percent of initial value, whichever is greater. $\Delta r_{DS(on)1}$ = ±20 percent of initial value, $\Delta V_{GS(th)1}$ = ±20 percent of initial value.	Subgroup 2 of table I herein; ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±25 µA dc or ±100 percent of initial value, whichever is greater. $\Delta r_{DS(on)1}$ = ±20 percent of initial value, $\Delta V_{GS(th)1}$ = ±20 percent of initial value.
14	Required.	Required.

(1) At the end of the test program, I_{GSSF1}, I_{GSSR1}, and I_{DSS1} are measured.
(2) An out-of-family program to characterize I_{GSSF1}, I_{GSSR1}, I_{DSS1}, and $V_{GS(th)1}$ shall be invoked.
(3) Shall be performed anytime before screen 9.

* 4.3.1. Screening (JANHC and JANKC). Screening of JANHC and JANKC die shall be in accordance with MIL-PRF-19500, "Discrete Semiconductor Die/Chip Lot Acceptance". As a minimum, die shall be 100 percent probed in accordance with table I, subgroup 2, except test current shall not exceed 20 A. Burn-in duration for the JANKC level follows JANS requirements; the JANHC follows JANTX requirements.

4.3.2 Gate stress test. Apply V_{GS} = 30 V minimum for t = 250 μs minimum.

4.3.3 Single pulsed unclamped inductive switching.

a. Peak current, I_D ..... I_{AR}(max).

b. Peak gate voltage, V_{GS} ..... 10 V.

c. Gate to source resistor, R_{GS} ..... $25 \leq R_g \leq 200\ \Omega$.

d. Initial case temperature ..... +25°C, +10°C, -5°C.

e. Inductance, L..... $\left[\frac{2E_{AS}}{(I_{D1})^2}\right]\left[\frac{(V_{BR}-V_{DD})}{V_{BR}}\right]$ mH minimum.

f. Number of pulses to be applied ..... 1 pulse minimum.

g. Supply voltage (V_{DD}) ..... 50 V, (25 V for devices with minimum $V_{(BR)DSS}$ of 100 V).

* 4.3.4 Thermal impedance ($Z_{\theta JC}$ measurements). The $Z_{\theta JC}$ measurements shall be performed in accordance with method 3161 of MIL-STD-750. The maximum limit (not to exceed the table I, subgroup 2 limit or figure 5 thermal impedance curve) for $Z_{\theta JC}$ in screening (table IV of MIL-PRF-19500) shall be derived by each vendor by means of statistical process control. When the process has exhibited control and capability, the capability data shall be used to establish the fixed screening limit. In addition to screening, once a fixed limit has been established, monitor all future sealing lots using a random five piece sample from each lot to be plotted on the applicable X bar R chart. If a lot exhibits an out of control condition, the entire lot shall be removed from the line and held for engineering evaluation and disposition. This procedure may be used in lieu of an in line monitor. The following parameter measurements shall apply:

a. I_M measuring current ..... 10 mA.

b. I_H drain heating current ..... 3 A minimum (5 A minimum for surface mount devices).

c. t_H heating time ..... 100 ms minimum (30 ms minimum for surface mount devices).

d. V_H drain-source heating voltage ... 25 V minimum (20 V minimum for surface mount devices).

e. t_{MD} measurement time delay ..... 30 to 60 μs.

f. t_{SW} sample window time ..... 10 μs maximum.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500. Alternate flow is allowed for conformance inspection in accordance with MIL-PRF-19500.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500, and table I herein. (End-point electrical measurements shall be in accordance with table I, subgroup 2 herein.)

* 4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table VIa (JANS) and table VIb (JAN, JANTX, and JANTXV) of MIL-PRF-19500 and as follows. Electrical measurements (end-points) and delta requirements shall be in accordance with table I, subgroup 2 herein.

4.4.2.1 Group B inspection, table VIa (JANS) of MIL-PRF-19500.

	Subgroup	Method	Conditions
	B3	1051	Test condition G.
*	B3	2075	See 3.4.2 herein.
	B3	2037	Test condition A. All internal wires for each device shall be pulled separately. If group B3 is to be continued to C6, strength test may be performed after C6.
	B4	1042	Test condition D, 2,000 cycles. The heating cycle shall be 1 minute minimum. No heat sink nor forced air cooling on the device shall be permitted during the on-cycle.
	B5	1042	A separate sample may be pulled for each test. Accelerated steady-state reverse bias; test condition A, V_{DS} = rated, T_A = +175°C, t = 120 hours, read and record $V_{BR(DSS)}$ (pre and post) at I_D = 1 mA. Read and record I_{DSS} (pre and post) in accordance with table I, subgroup 2 herein. $V_{BR(DSS)}$ delta cannot exceed 10 percent.
	B5	1042	Accelerated steady-state gate stress; test condition B, V_{GS} = rated, T_A = +175°C, t = 24 hours.
	B6		See 4.5.2.

4.4.2.2 Group B inspection, table VIb (JAN, JANTX, and JANTXV) of MIL-PRF-19500.

Subgroup	Method	Conditions
B2	1051	Test condition G.
B3	1042	Test condition D, 2,000 cycles. The heating cycle shall be 1 minute minimum. No heat sink nor forced air cooling on the device shall be permitted during the on-cycle.
B3	2037	Test condition A. All internal wires for each device shall be pulled separately. If group B3 is to be continued to C6, bond strength test may be performed after C6.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table VII of MIL-PRF-19500, and as follows. Electrical measurements (end-points) and delta requirements shall be in accordance with table I, subgroup 2 herein.

Subgroup	Method	Conditions
C2	2036	Test condition A; weight = 10 pounds, t = 15 s (not applicable for surface mount devices).
C5	3161	See 4.5.2.
C6	1042	Test condition D, 6,000 cycles. The heating cycle shall be 1 minute minimum. No heat sink nor forced air cooling on the device shall be permitted during the on-cycle.

* 4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in appendix E, table IX of MIL-PRF-19500 and as specified in table II herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.2 Thermal resistance. Thermal resistance measurements shall be performed in accordance with method 3161 of MIL-STD-750. $R_{\theta JC(max)}$ = .83°C/W for TO-254AA case style devices and surface mount devices. The following parameter measurements shall apply:

a. I_M measuring current .....10 mA.

b. I_H drain heating current.....3 A minimum (5 A minimum for surface mount devices).

c. t_H heating time .....Steady-state (see method 3161 of MIL-STD-750).

d. V_H drain-source heating voltage .....25 V minimum (20 V minimum for surface mount devices).

e. t_{MD} measurement time delay.....30 to 60 µs.

f. t_{SW} sample window time .....10 µs maximum.

* TABLE I. Group A inspection.

	Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
		Method	Conditions		Min	Max	
	Subgroup 1						
	Visual and mechanical inspection	2071					
	Subgroup 2						
*	Thermal impedance 2/	3161		$Z_{\theta JC}$		.65	°C/W
	Breakdown voltage, drain to source	3407	I_D = 1.0 mA dc, bias condition C, V_{GS} = 0 V dc	$V_{(BR)DSS}$			
	2N7224, 2N7224U				100		V dc
	2N7225, 2N7225U				200		V dc
	2N7227, 2N7227U				400		V dc
	2N7228, 2N7228U				500		V dc
	Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$ I_D = .25 mA	$V_{GS(th)1}$	2.0	4.0	V dc
*	Gate reverse current	3411	V_{GS} = +20 V dc, bias condition C, V_{DS} = 0	I_{GSSF1}		+100	nA dc
*	Gate reverse current	3411	V_{GS} = -20 V dc, bias condition C, V_{DS} = 0	I_{GSSR1}		-100	nA dc
	Drain current	3413	V_{DS} = 80 percent of rated V_{DS}, bias condition C, V_{GS} = 0	I_{DSS1}		25	µA dc
	Static drain to source on-state resistance	3421	V_{GS} = 10 V dc, condition A, pulsed (see 4.5.1), I_D = rated I_{D2} (see 1.3)	$r_{DS(on)1}$			
	2N7224, 2N7224U					0.070	Ohm
	2N7225, 2N7225U					0.100	Ohm
	2N7227, 2N7227U					0.315	Ohm
	2N7228, 2N7228U					0.415	Ohm
	Static drain to source on-state resistance	3421	V_{GS} = 10 V dc, pulsed (see 4.5.1), condition A, I_D = rated I_{D1} (see 1.3)	$r_{DS(on)2}$			
	2N7224, 2N7224U					0.081	Ohm
	2N7225, 2N7225U					0.105	Ohm
	2N7227, 2N7227U					0.415	Ohm
	2N7228, 2N7228U					0.515	Ohm

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 2 - Continued						
Forward voltage (source drain diode)	4011	Pulsed (see 4.5.1), $I_D = I_{D1}$ (see 1.3)	V_{SD}			
2N7224, 2N7224U					1.8	V
2N7725, 2N7225U					1.9	V
2N7227, 2N7227U					1.7	V
2N7228, 2N7228U					1.7	V
Subgroup 3						
High temperature operation:		$T_C = T_J = +125°C$				
Gate reverse current	3411	V_{GS} = +20 V dc and -20 V dc, bias condition C, V_{DS} = 0	I_{GSS2}		±200	nA dc
Drain current	3413	Bias condition C, V_{GS} = 0 V dc				
		V_{DS} = 80 percent rated	I_{DSS2}		0.25	mA dc
Static drain to source on-state resistance	3421	V_{GS} = 10 V dc, pulsed (see 4.5.1) I_D = rated I_{D2} (see 1.3)	$r_{DS(on)3}$			
2N7224, 2N7224U					0.11	Ohm
2N7225, 2N7225U					0.17	Ohm
2N7227, 2N7227U					0.68	Ohm
2N7228, 2N7228U					0.90	Ohm
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$ I_D = .25 mA dc	$V_{GS(th)2}$	1.0		V dc
Low temperature operation:		$T_C = T_J = -55°C$				
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, I_D = .25 mA dc	$V_{GS(th)3}$		5.0	V dc

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 4						
Switching time test	3472	I_D = rated I_{D2} (see 1.3), V_{GS} = 10 V dc, Gate drive impedance = 2.35 ohms; V_{DD} = 0.5 $V_{BR(DSS)}$				
Turn-on delay time			$t_{d(on)}$		35	ns
Rise time			t_r		190	ns
Turn-off delay time			$t_{d(off)}$		170	ns
Fall time			t_f		130	ns
Subgroup 5						
Safe operating area test	3474	See figure 6; V_{DS} = 80 percent of rated V_{DS} V_{DS} = 200 V maximum, t_p = 10 ms				
Electrical measurements		See table I, subgroup 2				
Subgroup 6						
Not applicable						
Subgroup 7						
Gate charge	3471	Condition B				
On-state gate charge			$Q_{g(on)}$			
2N7224, 2N7224U					125	nC
2N7225, 2N7225U					115	nC
2N7227, 2N7227U					110	nC
2N7228, 2N7228U					120	nC
Charge gate to source			Q_{gs}			
2N7224, 2N7224U					22	nC
2N7225, 2N7225U					22	nC
2N7227, 2N7227U					18	nC
2N7228, 2N7228U					19	nC

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 7 - Continued						
Charge gate to drain			Q_{gd}			
2N7224, 2N7224U					65	nC
2N7225, 2N7225U					60	nC
2N7227, 2N7227U					65	nC
2N7228, 2N7228U					70	nC
Reverse recovery time	3473	$V_{DD} \leq 30$ V, $d_i/d_t \leq 100$ A/µs $I_D = I_{D1}$	t_{rr}			
2N7224, 2N7224U					500	ns
2N7225, 2N7225U					950	ns
2N7227, 2N7227U					1,200	ns
2N7228, 2N7228U					1,600	ns

1/ For sampling plan, see MIL-PRF-19500.

* 2/ This test is required for the following end-point measurement only (not intended for 4.3, screen 9, 11, or 13): JANS, group B, subgroups 3 and 4; JAN, JANTX and JANTXV, group B, subgroups 2 and 3; group C, subgroup 6, and group E, subgroup 1.

* TABLE II. Group E inspection (all quality levels) for qualification or re-qualification only.

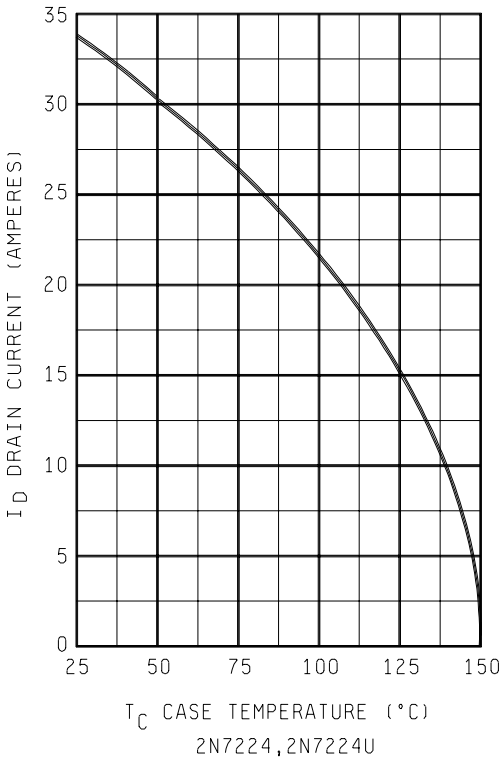
	Inspection 1/	MIL-STD-750		Sampling plan
		Method	Conditions	
	Subgroup 1			22 devices c = 0
	Temperature cycling	1051	500 cycles, test condition G	
	Electrical measurements		See table I, subgroup 2	
	Subgroup 2 2/			45 devices c = 0
	Steady-state reverse bias	1042	Condition A, 1,000 hours	
	Electrical measurements		See table I, subgroup 2	
	Steady-state gate bias	1042	Condition B, 1,000 hours	
	Electrical measurements		See table I, subgroup 2	
	Subgroup 3			3 devices c = 0
	DPA	2102		
	Subgroup 4			Sample size N/A
*	Thermal impedance curves		Each supplier shall submit their (typical) design maximum thermal impedance curves. In addition, the optimal test conditions and $Z_{\theta JX}$ limit shall be provided to the qualifying activity in the qualification report	
	Subgroup 5 3/			
	Barometric pressure (reduced) 2N7227, 2N7227U 2N7228, 2N7228U	1001	Condition C, $V_{(ISO)} = V_{DS}$	15 devices c = 0
	Subgroup 6			3 devices
*	ESD	1020	Not required for devices classified as ESD class 1.	

See footnotes at end of table.

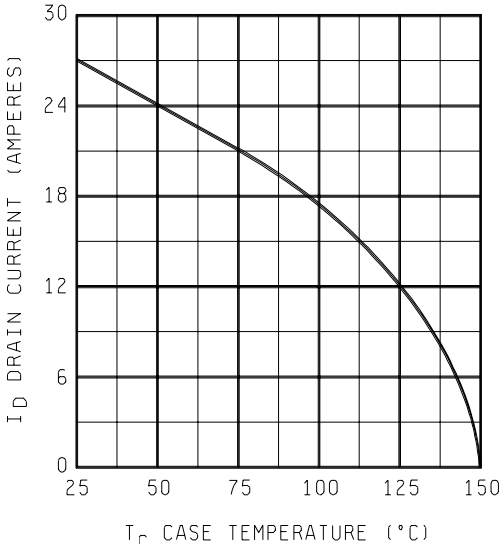
* TABLE II. Group E inspection (all quality levels) for qualification or re-qualification only - Continued.

	Inspection 1/	MIL-STD-750		Sampling plan
		Method	Conditions	
*	Subgroup 8			5 devices, c = 0
	Repetitive avalanche energy	3469	Peak current $I_{AR} = I_D$; peak gate voltage V_{GS} = 10 V; gate to source resistor, R_{GS} 2.5 ≤ R_{GS} ≤ 200 ohms, temperature = T_J = +150°C +0, -10°C Inductance = $\left[\frac{2E_{AR}}{(I_{D1})^2}\right]\left[\frac{V_{BR}-V_{DD}}{V_{BR}}\right]$ $mH\,\min$ Number of pulses to be applied = 3.6 X 10^8; supply voltage (V_{DD}) = 50 V; time in avalanche = 2 µs minimum, 20 µs minimum; f = 500 Hz minimum	
*	Subgroup 9			22 devices, c = 0
	Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476		

1/ JANHC and JANKC device are qualified with MIL-PRF-19500.
2/ A separate sample for each test may be pulled.
3/ Not required for 2N7224, 2N7224U, 2N7225, and 2N7225U.

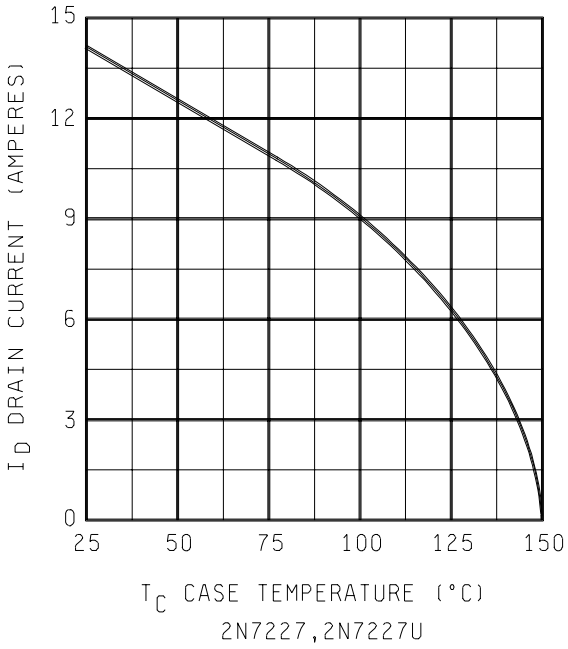


2N7224, 2N7224U



2N7225, 2N7225U

* FIGURE 4. Maximum drain current vs case temperature.



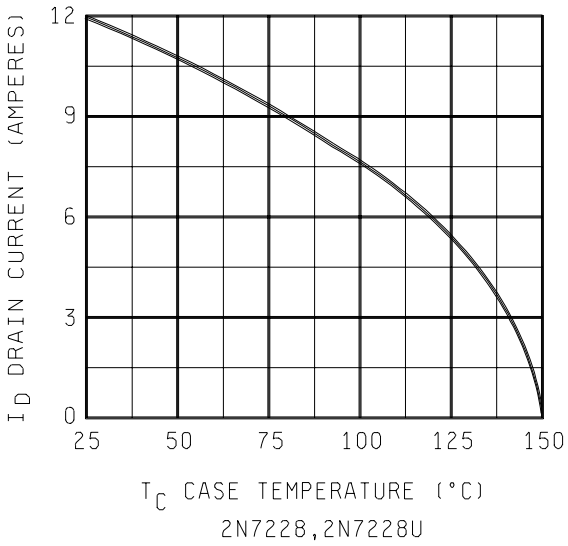


FIGURE 4. Maximum drain current vs case temperature - Continued.

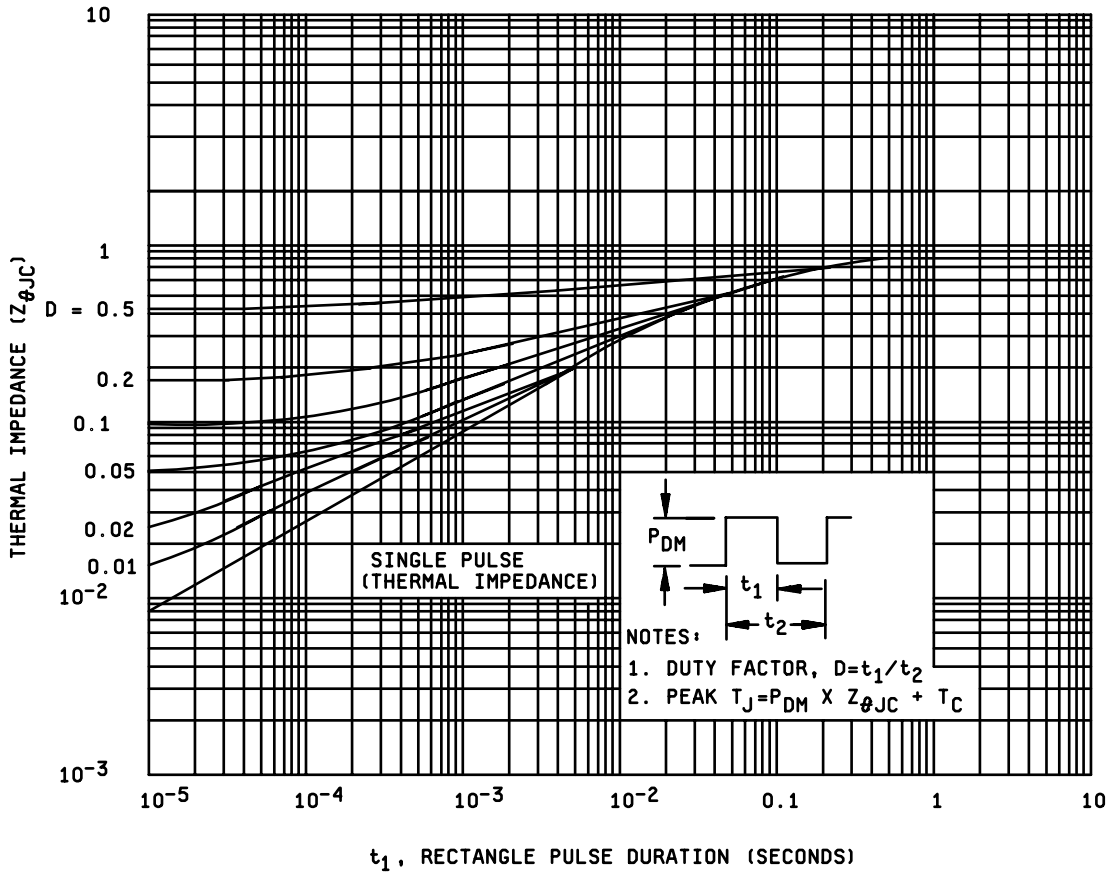
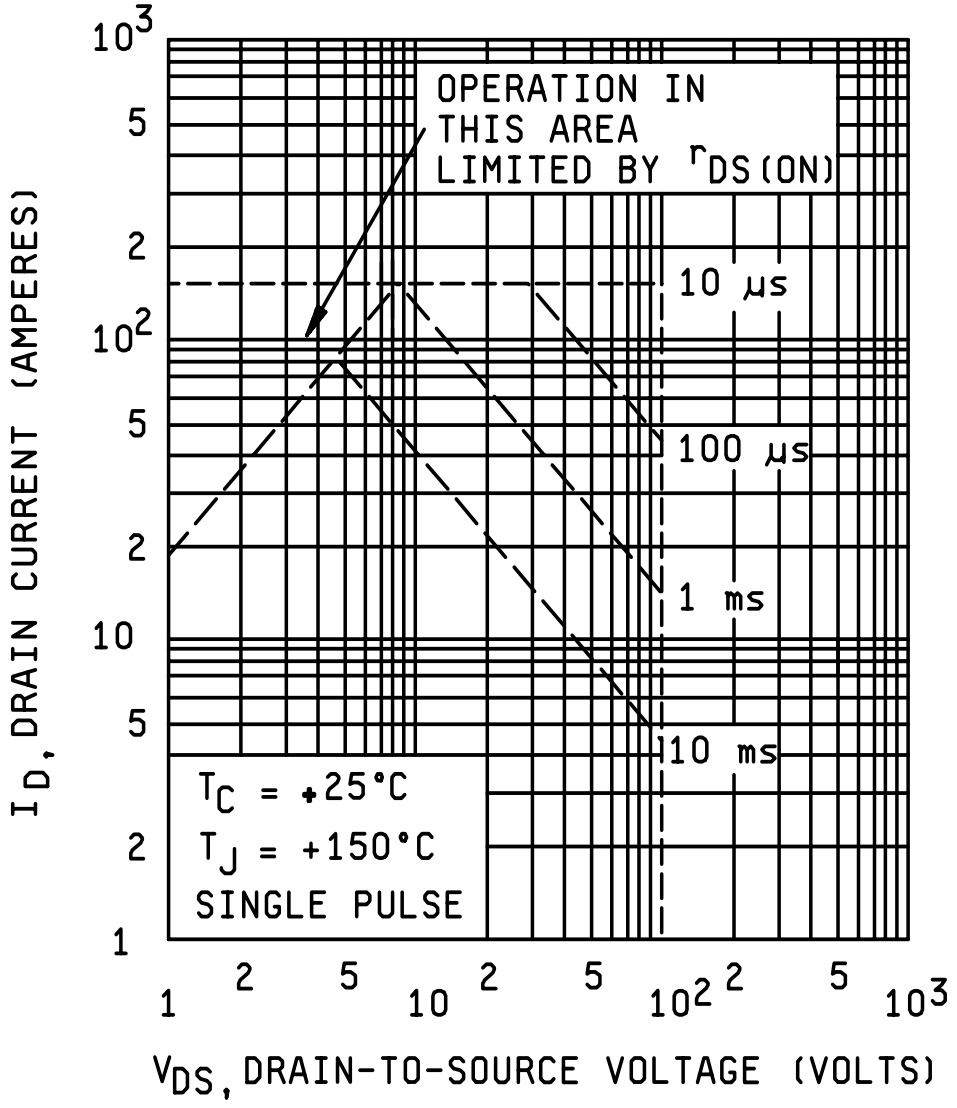
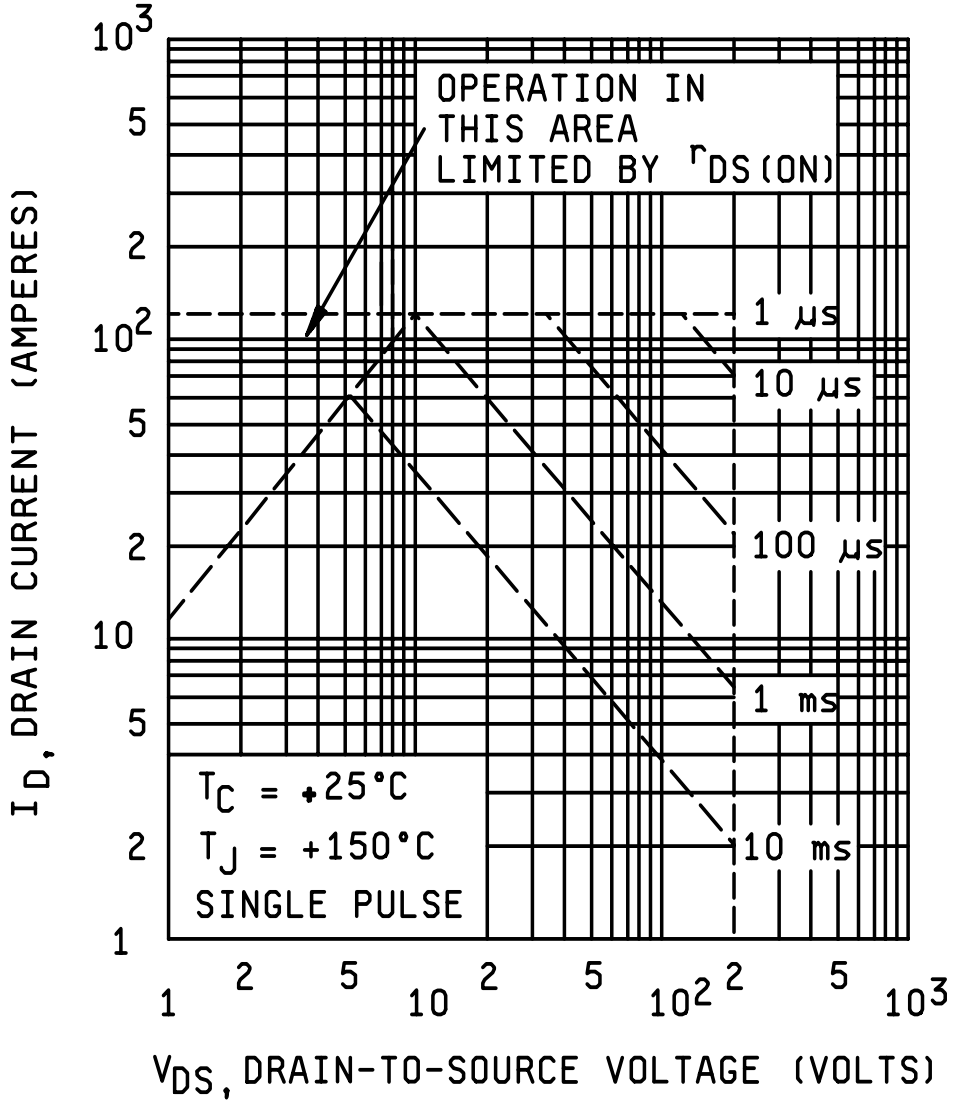


FIGURE 5. Thermal impedance curves.



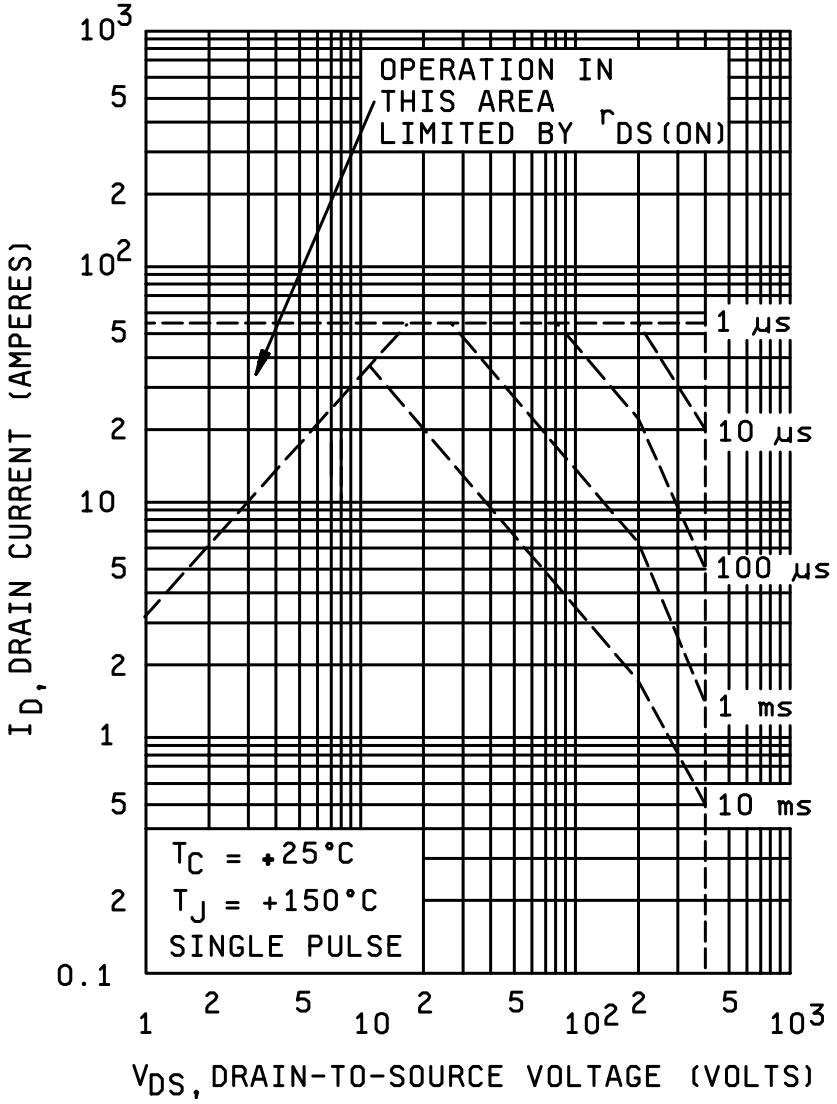
2N7224, 2N7224U

FIGURE 6. Safe operating area graph.



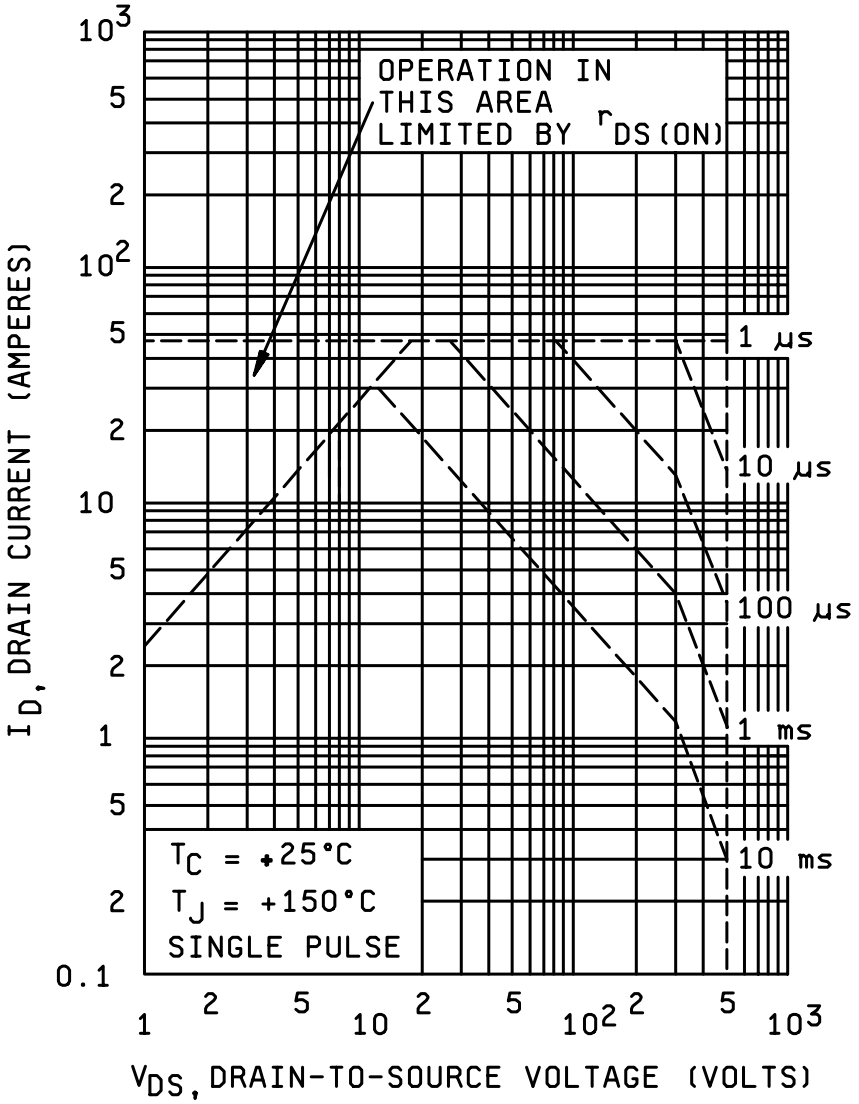
2N7225, 2N7225U

FIGURE 6. Safe operating area graph - Continued.



2N7227, 2N7227U

FIGURE 6. Safe operating area graph - Continued.



2N7228, 2N7228U

FIGURE 6. Safe operating area graph - Continued.

5. PACKAGING

* 5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When actual packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Notes. The notes specified in MIL-PRF-19500 are applicable to this specification.

* 6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.1).

d. Product assurance level and type designator.

* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from Defense Supply Center, Columbus, ATTN: DSCC/VQE, P.O. Box 3990, Columbus, OH 43216-5000 or e-mail vqe.chief@dla.mil.

6.4 Supersession and substitution of DESC drawing. This specification supersedes DESC drawing 89026, dated 19 December 1989.

6.5 Suppliers of die. The qualified die suppliers will be identified on the QML (example JANHCA7224).

JANC ordering information		
Military PIN	Manufacturer	
	59993	59993
2N7224 2N7225 2N7227 2N2778	JANHCA2N7224 JANHCA2N7225 JANHCA2N7227 JANHCA2N7228	JANKCA2N7224 JANKCA2N7225 JANKCA2N7227 JANKCA2N7228

6.6 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 11
NASA - NA
DLA - CC

Review activities:
Army - AR, MI
Navy - TD
Air Force - 70, 99

Preparing activity:
DLA - CC

(Project 5961-2872)

* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at http://www.dodssp.daps.mil .